Amendments to the Specification

Page 26, lines 12-23: Replace the paragraph with the following new paragraph:

Furthermore, in the first drive transformer control circuit 200, a second resistance 27, a second capacitor 28, a second diode 29 and a ~~second~~ first n-channel FET 30 are provided. The first n-channel FET 30 is ON/OFF-driven according to the input first PWM signal VG1. In the first drive transformer control circuit 200, the configuration is such that the turn-on of the first n-channel FET is delayed by the second resistance 27 and the second capacitor 28. The turn-off thereof is carried out without delay.

Page 27, lines 17-26 and, Page 28 lines 1-2: Replace the paragraph with the following new paragraph:

In the second drive transformer control circuit 201, a third resistance 37, a sixth capacitor 38, a fifth diode 39 and a second p-channel FET 40 are provided. The ~~first n~~ second p-channel FET 40 is ON/OFF-driven according to the input second PWM signal VG2. In the second drive transformer control circuit 201, the configuration is such that the turn-on of the ~~first n~~ second p-channel FET 40 is delayed by the third resistance 37 and the sixth capacitor 38. The turn-off thereof is carried our without delay via the fifth diode 39.

Page 28, lines 3-14: Replace the paragraph with the following new paragraph:

Furthermore, in the second drive transformer control circuit 201, a ~~forth~~ fourth resistance 41, a seventh capacitor 42, a sixth diode 43 and a second n-channel FET 44 are provided. The second n-channel FET 44 is ON/OFF driven according to the input second PWM signal VG2. IN the second drive transformer control circuit 201, the configuration is such that the turn-on of the second n-channel FET 44 is delayed by the fourth resistance 41 and the seventh capacitor 42. The turn-off thereof is carried out without delay.

Page 34, Lines 22-26, and Page 35, Lines 1-15: Replace the paragraph with the following new paragraph:

When the first n-channel FET 30 is turned OFF in synchronism with the falling edge of the drive signal VG1, by the energy stored in the primary winding 32a of the first drive transformer 32, the gate capacitance of the first synchronous rectifier device 8 is charged, and the

first synchronous rectifier device 8 is turned ON. When the drain voltage of the first p-channel FET 26 increases to the output voltage of the auxiliary power supply 14, the body diode of the first p-channel FET 26 is turned ON, and the exciting current of the first drive transformer 32 is regenerated to the side of the auxiliary power supply. The first p-channel FET 26 is ~~tuned~~ turned ON after a slight delay so as to be placed into the ON state after the gate capacitance of the first synchronous rectifier device 8 is fully charged, so that the charge current is not supplied from the side of the auxiliary power supply.